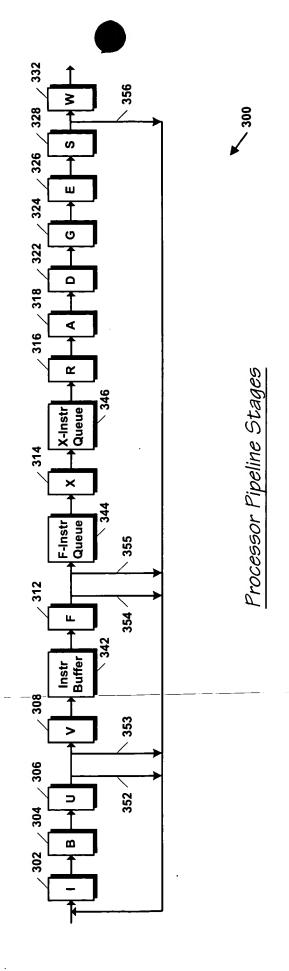
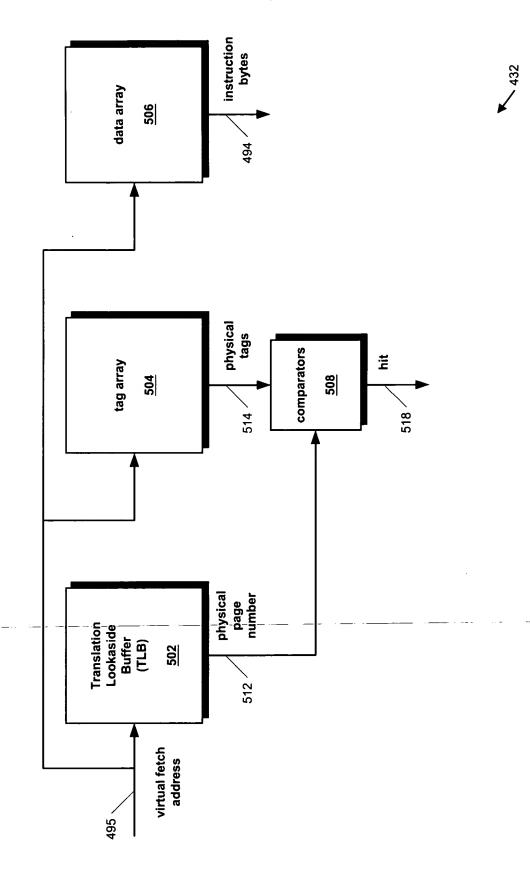


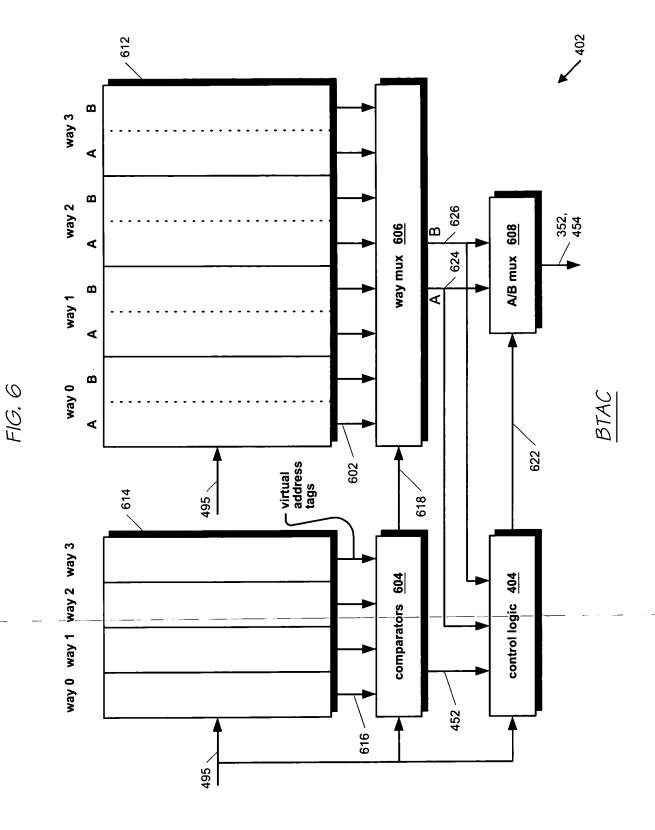
F1G. 3



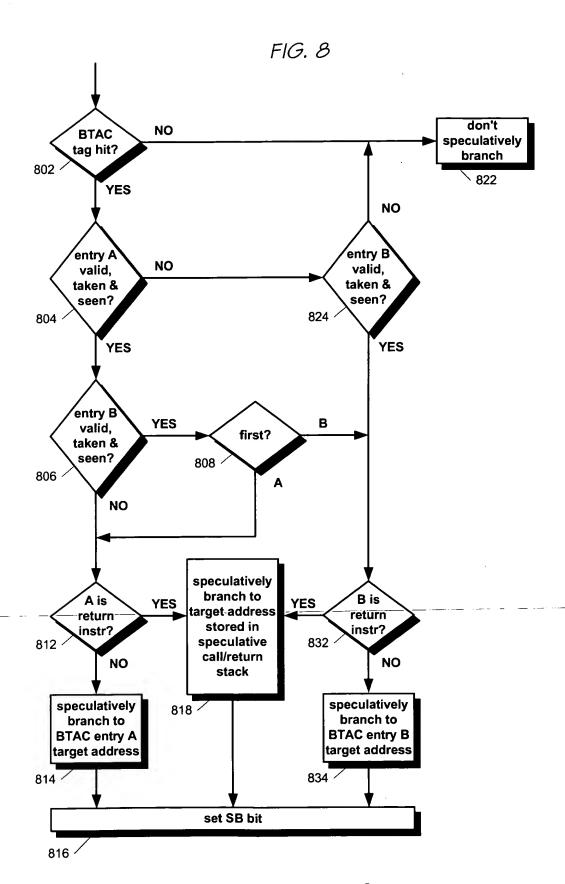
F1G. 5



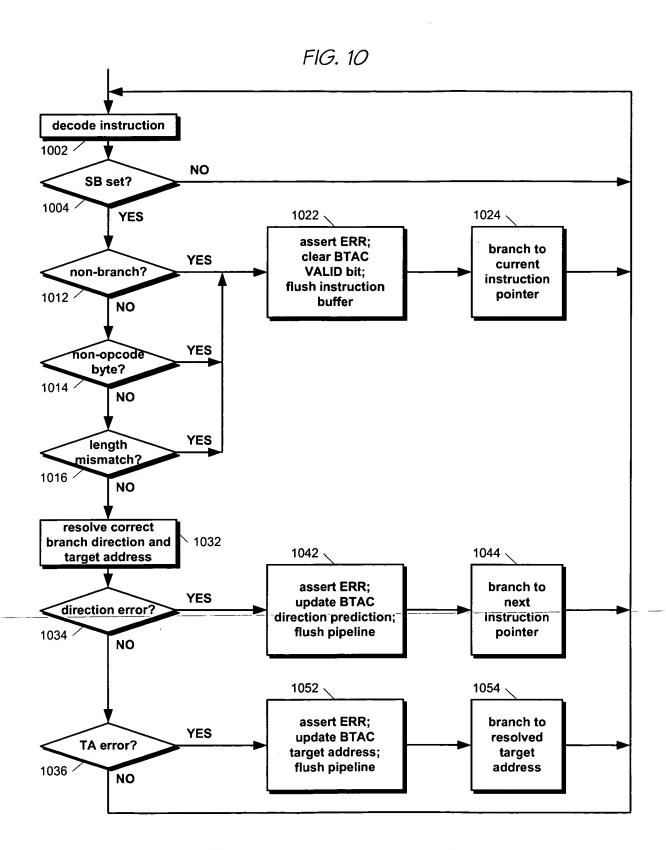
Instruction Cache



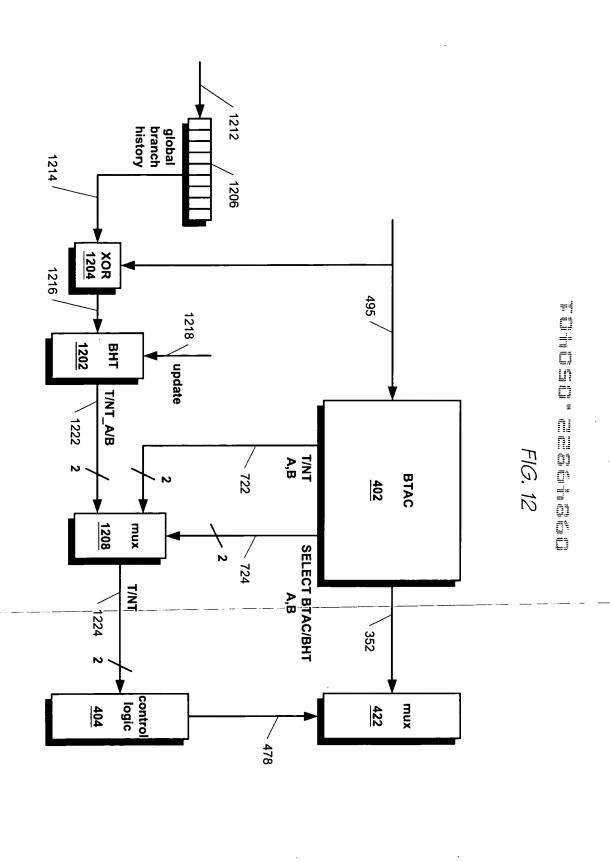
) 714		iction Information 712		√
target address (TA) 714	······································	Branch Direction Prediction Information (BDPI) 712		
	••••••	WRAP 708	SELECT 724	7 V T T V T T V T T T T T T T T T T T T
		RET 706	6	и Р
		CALL 704	T/NT 722	
speculative branch information (SBI) 454		LEN 448	`.	
		BEG 446		
sculative bra		VALID 702		



Speculative Branching Operation



<u>Detection and Correction of</u> Speculative Branch Misprediction



Hybrid Speculative Branch Direction Predictor

1200

11.017

Previous Code Sequence:

0x00000010 JMP 0x00001234

Current Code Sequence:

0×0000153¢ INC 0×0000153¢

X	X	ααΑ					F-stage
X	X	X	QQA				9gst≥-V
X	X	X	X	ΔΦΑ			U-stage
X	X	aus	X	X	ADD		B-stage
QQA	X	INC	ans	X	X	adA	l-stage
L	9	S	Þ	3	2	l l	Clock →

Cycle 1 = BTAC and I-cache access cycle

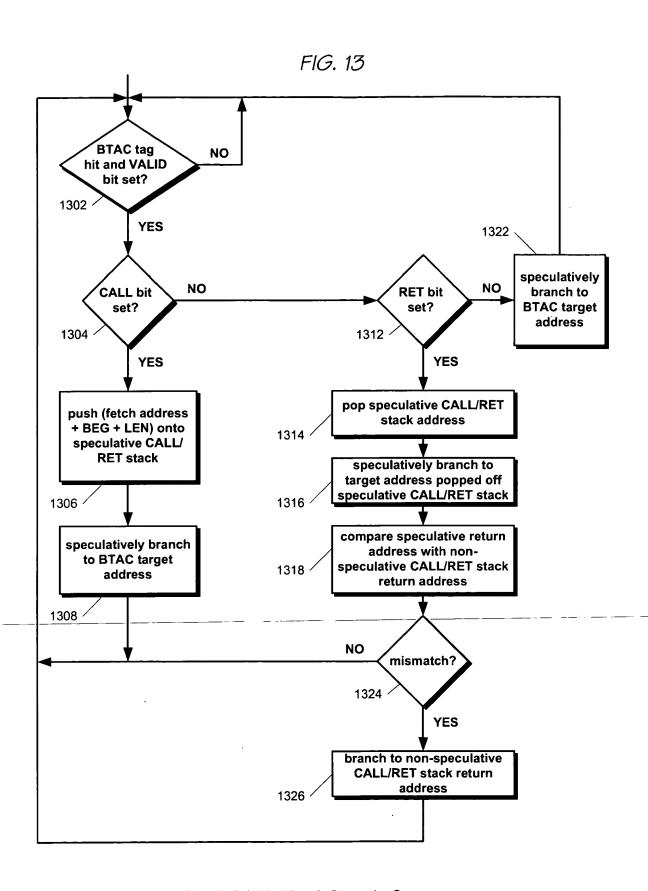
Cycle 4 = speculative branch cycle

Cycle 5 = speculative branch error detection cycle

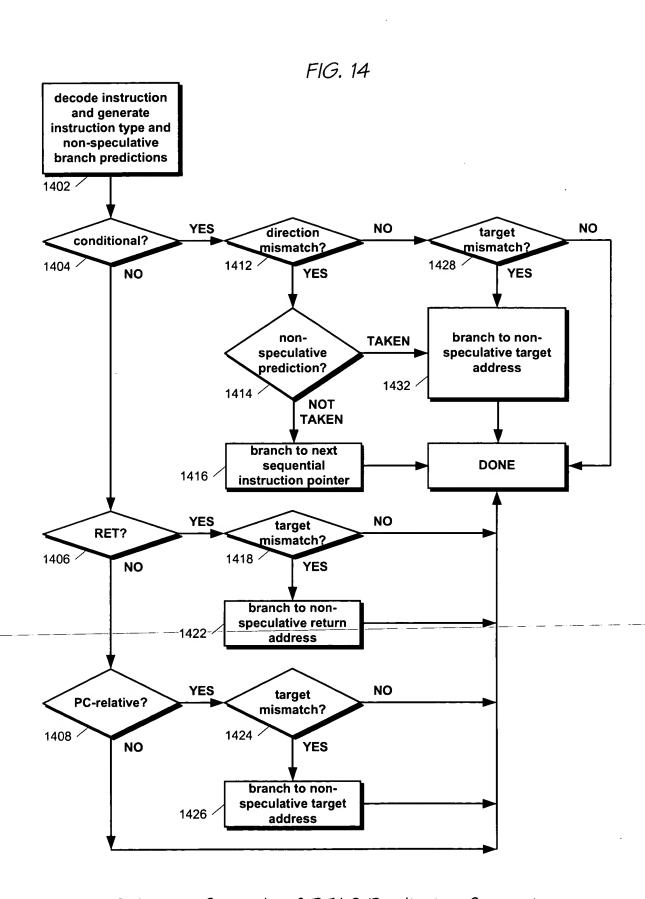
Cycle 6 = BTAC invalidate cycle Cycle 7 = speculative branch error correction cycle

1100

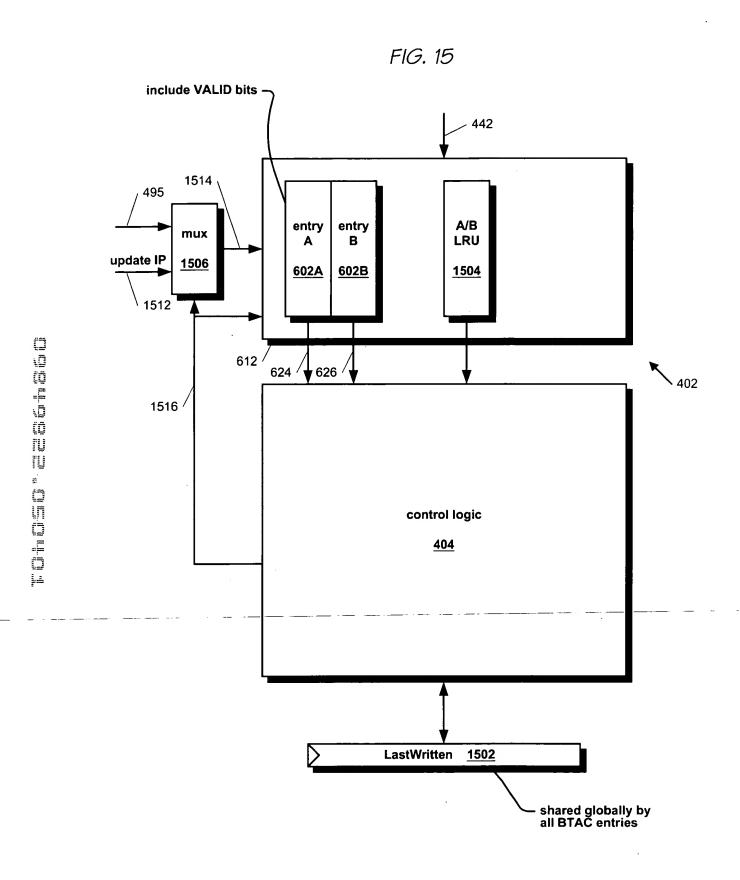
Misprediction Detection and Correction Example



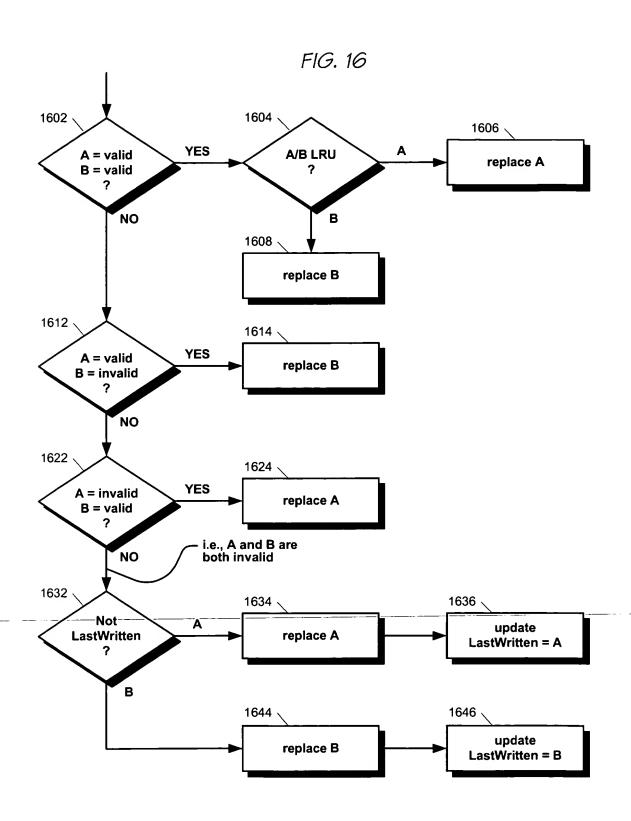
Dual CALL/RET Stack Operation

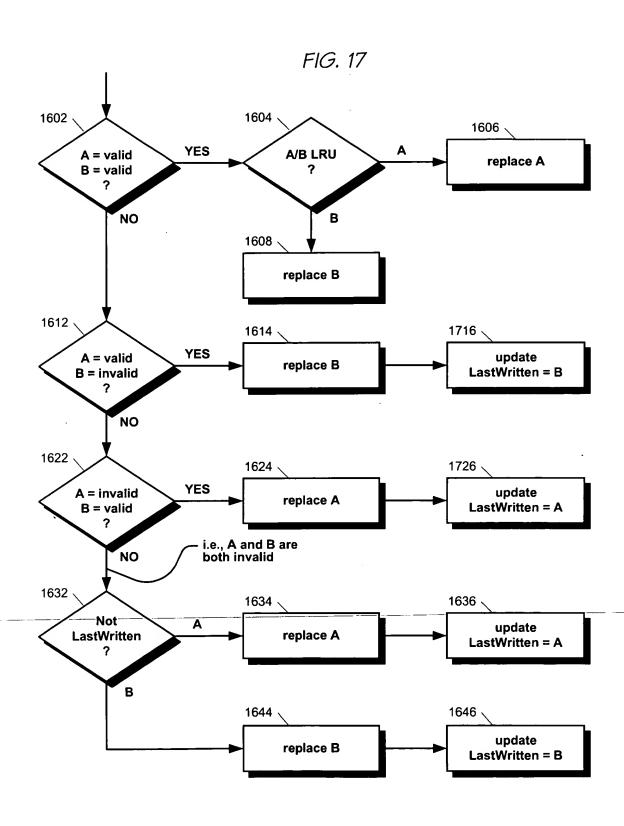


Selective Override of BTAC Prediction Operation



BTAC A/B Replacement Apparatus

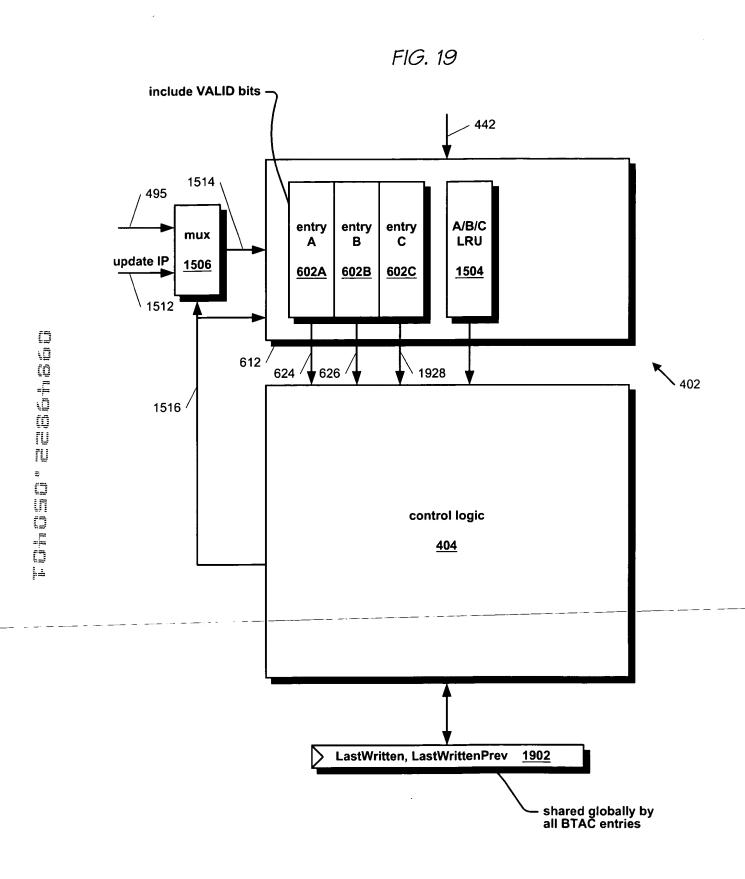




A/B Entry Replacement Method (Alt. Embodiment)

FIG. 18 include VALID bits; don't include T/NT bits single-ported dual-ported 442 1842 1514 495 A/B T/NT T/NT entry entry mux В LRU Α В update IP <u>1506</u> 602A 602B <u>1504</u> 722A 722B 1512 1812 / 612 624 / 626 402 1516 control logic <u>404</u> LastWritten 1502 shared globally by all BTAC entries

BTAC A/B Replacement Apparatus (Alt. Embodiment)



BTAC A/B/C Replacement Apparatus